LISTING OF CLAIMS

1. (original) A method for detecting a mismatch in a content addressable memory (CAM), the method comprising:

charging a matchline of a match detection circuit of said CAM to a first voltage level;

comparing a logic state of a first bit stored in said CAM with a logic state of a second bit received at said CAM; and

changing the voltage level of said matchline to a second voltage level if the logic state of the first bit does not match the logic state of the second bit, said second voltage level being different than said first voltage level and different than a ground potential.

2. (original) The method of claim 1, wherein said act of charging comprises:

precharging said matchline to said first voltage level before said second bit is received at said CAM.

3. (original) The method of claim 2, wherein said act of precharging comprises precharging said matchline to VDD.

4. (original) The method of claim 2, wherein said act of precharging comprises precharging said matchline to a negative reference voltage level lower than VDD.

5. (original) The method of claim 1, wherein said act of comparing comprises:

comparing said logic state of said first bit with a logic state of a complement of said second bit; and

comparing a logic state of a complement of said first bit with said logic state of said second bit.

6. (original) The method of claim 5, wherein said first act of comparing comprises:

receiving said logic state of said first bit at a gate of a first transistor; and

receiving said logic state of said complement of said second bit at a gate of a second transistor in series with said first transistor, wherein if said logic state of said first bit matches said complement of said logic state of said second bit, said first and second transistors are activated and conducting.

7. (original) The method of claim 5, wherein said second act of comparing comprises:

receiving said logic state of said complement of said first bit at a gate of a third transistor; and

receiving said logic state of said second bit at a gate of a fourth transistor in series with said third transistor, wherein if said logic state of said complement of said first bit matches said logic state of said second bit, said third and fourth transistors are activated and conducting.

8. (original) The method of claim 6, wherein said act of changing comprises coupling said matchline, via said first and second transistors, to a terminal having a voltage level lower than said first voltage level and a voltage level higher than a ground potential.

9. (original) The method of claim 7, wherein said act of changing comprises coupling said matchline, via said third and fourth transistors, to a terminal having a voltage level lower than said first voltage level and a voltage level higher than a ground potential.

10. (original) A method for detecting a mismatch in a content addressable memory (CAM), the method comprising:

charging a matchline of a match detection circuit of said CAM to a first voltage level;

respectively comparing logic states of a first plurality of bits stored in said CAM with respective logic states of a second plurality of bits received at said CAM, each of said second plurality of bits having a corresponding bit in said first plurality of bits; and

changing the voltage level of said matchline to a second voltage level if the logic state of at least one of said second plurality of bits does not match the logic state of its corresponding bit in said first plurality of bits, said second voltage level being different than said first voltage level and higher than a ground potential.

11. (original) The method of claim 10, wherein said act of charging comprises:

precharging said matchline to said first voltage level before said second plurality if bits is received at said CAM.

12. (original) The method of claim 11, wherein said act of precharging comprises precharging said matchline to VDD.

Claims 13-54 (canceled)